In the Abstract

Please amend the ABSTRACT OF THE DISCLOSURE of this application as follows:

--A Booth encoding circuit includes a plurality of cells (202a-202d), in which at least one of the cells (202c) includes a plurality of inputs. The cell also includes a first plurality of transistors ~~(203), which form~~ (203) receiving at least one input and forming a ~~first~~ NAND logic stage~~, in which at least one of the inputs is connected to at least one of the first plurality of transistors (203)~~. The cell further includes a second plurality of transistors ~~(211), which form~~ (211) receiving at least one input and forming ~~a second~~ an OR logic stage~~, in which at least one of the inputs is connected to at least one of the second plurality of transistors (211)~~. The cell also includes a first output inverter (222) connected to at least one of the second plurality of transistors (211), and a first switching means (224) connected to at least one of the first plurality of transistors (203). The cell further includes a second switching means (226) connected to the first output inverter (222), and a second output inverter (228) connected to the first switching means (224) and the second switching means (226). ~~Moreover, within a critical path of the Booth encoding circuit, the first output inverter (222) drives the second output inverter (228). In one embodiment, the first output inverter (222) drives the second output inverter (228) via the second switching means (226).~~--